ABSTRACT

A bridge device for use in computer systems has a first interface to a first interconnect apparatus such as a processor bus. It also has a second interface to second interconnect apparatus such as an I/O bus. The second interconnect apparatus is of a type capable of connection to a DMA-capable peripheral device. The bridge device has address translation hardware to translate I/O virtual addresses received from the second interface into physical memory addresses for transmission onto the first interface. The address translation hardware has an associated coherency maintenance apparatus. In a particular embodiment, the address translation hardware has a translation lookaside buffer and the coherency maintenance apparatus is apparatus for snooping through the first interface, invalidating TLB entries when a page table in memory is updated.